Duration: 08:30 - 17:50
Room: Prag

WS-06
Integration of III-V Nanowire Semiconductors for Next Generation High Performance CMOS SOC Technologies and Competitive Solutions

Organisers:
Lars-Erik Wernersson, Lund University, Sweden
Didier Belot, CEA-LETI, France

Abstract
III-V nanowires are attractive for scaled transistors at future electronics nodes. The advantageous transport properties of III-V materials, combined with the improved electrostatic control of nanowire structures, allows for aggressive scaling of the gate length. In addition, the reduced dimension eases the path for integration of III-V materials on a Si platform, reducing cost and saving on scarce minerals. The introduction of a gate dielectric reduces the leakage current and assists in further scaling of III-V MOSFET channel lengths below the current limitations of III-V HEMT technologies. Currently the III-V nMOSFETs have demonstrated very high Ion for digital applications as well as very high gm. Objective of this workshop is to underline initiatives which aims at exploiting the transistor benefits in the millimetre wave application area. We will focus on key circuits including both LNAs and PAs. Co-integration of III-V technology with Si CMOS as well as all-III-V CMOS technology is considered. In this workshop, we will discuss the benefits of the III-V nanowire technology and compare to other available technologies. We will demonstrate very high performance on the transistor level and present the most promising approaches to exploit the transistor properties at the circuit level. The workshop will start with an overview of the state of art, and initiatives targeting III-V integration in Si technologies, followed by a presentation focusing on trends in RF and mmW applications which are demanding new developments for high performance devices. The workshop will also provide a complete overview from materials, through devices to full circuit design and circuit evaluation. Presentations from “best in class” European researchers active in the area of III-V materials, devices and circuits, will provide a European Perspective on the current state of the art in III-V devices for RF and mmW applications. At the end of the day, a round table discussion will close the workshop, in order to well define which technology can answer to which application.

Programme

08:30 - 08:55 Introduction
Lars-Erik Wernersson, University of Lund, Sweden

08:55 - 09:20 Application Trends and Technology Needs
Sven Mattisson, Ericsson, Sweden

09:20 - 10:10 Material for III-V Nanowires
Iain Thayne, University of Glasgow, UK

10:10 - 10:50 Break

10:50 - 11:40 IIII-V Materials and Devices for RF and mm-Wave Research
Nadine Collaert, IMEC, Belgium

11:40 - 12:30 Devices and Modeling for RF and mm-Wave
Michael Schröter, University of Dresden, Germany

12:30 - 13:50 Break

13:50 - 14:40 Devices and Modeling
Erik Lind, University of Lund, Sweden

14:40 - 15:30 III-V CMOS Co-Integration
Veeresh Deshpande, IBM, Switzerland

15:30 - 16:10 Break

16:10 - 16:50 III-V and Si Circuits for RF and mm-Wave
Herbert Zirath, Chalmers University, Sweden

16:50 - 17:30 III-V CMOS Circuit for RF and mm-Wave
Thomas Merkle, Fraunhofer, Germany

17:30 - 17:50 Round Table Discussion and Conclusion
Moderator: Didier Belot, LETI, France